AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions and listings of Claims in the subject Patent Application:

Listing of Claims:

Claim 1 (Currently amended) A circuit structure for a serial Advanced Technology Attachment (ATA) ~~ATA~~ external physical layer comprising:

a decoder/encoder connected to a storage medium controller via a set of parallel signal transmission lines and a set of parallel signal receiving lines for decoding a parallel transmission signal originated from said storage medium controller into a parallel transmission data signal and at least one control signal ~~signals~~;

at least one serializer/deserializer connected to said decoder/encoder for the conversion of said parallel transmission data signal into a serial transmission data signal;

at least one phase locked loop connected to said decoder/encoder and ~~said~~ at least one serializer/deserializer, respectively, for receiving said at least one control signal ~~signals~~ originated from ~~form~~ said decoder/encoder, as well as generating clock signals required for the operation of said physical layer and transmitting a reference clock signal to said storage medium controller;

a plurality of ~~at least one~~ transmitters, connected to said serializer/deserializer, each of said transmitters being used to transmit said serial transmission data signal to a serial ATA device connected thereto via a set of serial signal transmission lines;

a plurality of ~~at least one~~ receivers connected to said serializer/deserializer, each of said receivers being used to transmit a serial receiving data signal received from said serial ATA

device connected thereto to said serializer/deserializer, and then said serial receiving data signal being converted into a parallel receiving data signal by said serializer/deserializer for transmitting to said decoder/encoder; and

at least one out of band (OOB) ~~OOB~~ signal detector ~~detectors~~ connected to receiving signal lines of said corresponding receivers, respectively, for detecting the operation condition of said serial ATA device and transmitting at least one set ~~sets~~ of detected status signals to said decoder/encoder, said parallel receiving data signal and said status signals then being encoded into a parallel receiving signal by said decoder/encoder and, afterward, transmitted to said storage medium controller via said set of parallel signal receiving lines.

Claim 2 (original) The circuit structure according to Claim 1, wherein said decoder/encoder comprise a decoder and an encoder, said decoder being connected to said storage medium controller via said set of parallel signal transmission lines, and said encoder being connected to said storage medium controller via said set of parallel signal receiving lines.

Claim 3 (Currently amended) The circuit structure according to Claim 1, wherein said serializer/deserializer comprises at least one serializer ~~serializers~~ and at least one deserializer ~~deserializers~~.

Claim 4 (Currently amended) The circuit structure according to Claim 3, wherein ~~a~~ an elastic buffer is provided between ~~each of~~ said at least one deserializer ~~deserializers~~ and said decoder/encoder.

Claim 5 (Currently amended) The circuit structure according to Claim 1, wherein said at least one phase locked loop comprises at least one transmission phase locked loop and at least one receiving phase locked loop.

Claim 6 (Currently amended) The circuit structure according to Claim 1, wherein said at least one control signal comprises ~~signals comprise~~ reset signals, power control signals, transmission valid signals, and one of the combinations thereof.

Claim 7 (Currently amended) The circuit structure according to Claim 6, wherein said at least one control signal ~~signals~~ further comprises ~~comprise~~ control signals and receiving rate control signals.

Claim 8 (original) The circuit structure according to Claim 1, wherein said status signals comprise communication initialization signals, communication wake up signals, receiving squelch signals, receiving phase lock loop ready signals, and one of the combinations thereof.

Claim 9 (Currently amended) The circuit structure according to Claim 1, wherein said at least one phase locked loop has a function of transmission rate switching.

Claim 10 (Currently amended) The circuit structure according to Claim 1, further comprising a power controller for controlling the reset and other power states of said physical layer and connected serial ATA devices.

Claim 11 (Currently amended) The circuit structure according to Claim 3, further comprising at least one selector ~~selectors~~, one input ~~of each~~ of which being connected to said at least one serializer, the other input thereof being connected to said at least one receiver, and an output thereof ~~may be~~ being connected to said at least one deserializer.

Claim 12 (Currently amended) The circuit structure according to Claim 1, wherein said circuit structure is capable of being integrated into a chip.

Claim 13 (Currently amended) The circuit structure according to Claim 1, wherein only one integrated drive electronics (IDE) ~~IDE~~ bus is needed for ~~connecting to~~ connection between said physical layer and said storage medium controller.

Claims 14-19 (cancelled).